Abstracts

Attenuation Compensation in Distributed Amplifier Design

S. Deibele and J.B. Beyer. "Attenuation Compensation in Distributed Amplifier Design." 1989 Transactions on Microwave Theory and Techniques 37.9 (Sep. 1989 [T-MTT] (Special Issue on FET Structures Modeling and Circuit Applications)): 1425-1433.

A high-gain common-gate FET can present at its drain a broad-band impedance characterized by a (frequency-dependent) negative resistance and a capacitance. This is examined both theoretically and experimentally. Loading the input and/or the output lines of a distributed amplifier with this circuit reduces the signal losses, leading to an increase in the allowed number of active devices with a consequent increase in the gain-bandwidth and gain-maximum frequency products. The cascode circuit, a related loss reduction network, is also evaluated because of its use in distributed amplifiers. Several designs employing the common-gate FET loss-compensating circuit and/or the cascode amplifying circuit are compared to a conventional distributed amplifier optimized for gain-bandwidth product. Simulated gain-maximum operating frequency product increases of 27 to 245 percent over that of the optimized conventional distributed amplifier are shown. The increase in single-stage amplifier gain provided by this technique often results in (proportionally) higher maximum output power.

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